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Plasma CVD of $(BaSr)TiO_3$ Dielectrics for Gigabit DRAM Capacitors

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Abstract. Electron cyclotron resonance (ECR) plasma chemical vapor deposition (CVD) of $(BaSr)TiO_3$ dielectrics is reviewed. The oxygen plasma lowered the crystallization temperature and carbon contamination. $(BaSr)TiO_3$ CVD process was developed under conditions of relatively low deposition rate of 1.1 nm/min and a relatively low deposition temperature of 550°C. Utilizing this process, we developed a gigabit dynamic random access memory (DRAM) capacitor technology involving the preparation of a thin $(BaSr)TiO_3$ capacitor dielectric over a RuO_2/Ru storage node contacting a TiN/$TiSi_x$/poly-Si plug. The ECR plasma CVD enabled uniform deposition of gigabit-DRAM-quality $(BaSr)TiO_3$ films on the electrode sidewalls. The storage node contact improved in endurance against oxidation, by fabricating the buried-in TiN/$TiSi_x$/poly-Si plug (TiN-capped plug) under the RuO_2/Ru storage node. $(BaSr)TiO_3$ films with a small equivalent SiO_2 thickness of 0.38 nm and a leakage current density of 8.5×10^{-7} A/cm^2 at an applied voltage of 1.0 V, were obtained without any further annealing process. An equivalent SiO_2 thickness of 0.40 nm on the RuO_2 sidewall was also achieved. It is concluded that this technology has reached the requirements for gigabit DRAM capacitors.

Keywords: (BaSr) TiO_3, dielectrics, plasma CVD, giga-bit DRAM, DRAM cell capacitor, capacitor integration

Introduction

Higher integration of dynamic random access memories (DRAMs) is the ''technology driver'' of all Si semiconductor devices. DRAMs had gone to the megabit prototype stage in 1985 [1]. They have now entered the gigabit era in research and development fields [2,3]. In the development of capacitor dielectrics, the application of high-dielectric-constant (high-permittivity) materials has been investigated to maintain sufficient memory-cell capacitance in the ultralarge scale integration. One dielectric material for this application is $(BaSr)TiO_3$ [4]. This dielectric has the most stable characteristics among high-dielectric-constant paraelectric materials at operating temperatures [5] and frequencies [6]. Thin $(BaSr)TiO_3$ film deposition methods for DRAM cell capacitors include sputtering [4,7–9] and chemical vapor deposition (CVD) [10–14].

While many sputtered $(BaSr)TiO_3$ films [5,15–17] have shown superior performance characteristics, their film coverage over storage nodes tends to be insufficiently uniform. This drawback is particularly disadvantageous in capacitor integration because simple three-dimensional storage nodes are still necessary to apply $(BaSr)TiO_3$ for gigabit DRAM capacitors [12,13]. For conformality, CVD methods [18–21] are more appropriate. Their deposition temperatures are sufficiently low (< 500°C) to form conformal $(BaSr)TiO_3$ films. And these $(BaSr)TiO_3$ films are crystallized by subsequent high temperature annealing.

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$SrTiO_3$ and $(BaSr)TiO_3$ dielectrics were obtained at a relatively low deposition temperature by electron cyclotron resonance (ECR) plasma CVD [22–27]. These dielectric thin films have been deposited on the various storage nodes consisting of RuO_2 for DRAM cell capacitor application [12–14]. Consider the situation, in which gigabit-DRAM-quality $(BaSr)TiO_3$ films are obtained at the lower temperature of T_l and storage nodes with the contact plug endure the oxidation at the higher temperature of T_h. In the situation where T_h is higher than T_l, we have a solution to the $(BaSr)TiO_3$ capacitor integration.

This paper describes ECR plasma CVD of $(BaSr)TiO_3$ dielectrics and its application to a capacitor integration technology involving the preparation of $(BaSr)TiO_3$ over a RuO_2/Ru storage node contacting a buried-in TiN/$TiSi_x$/poly-Si plug (TiN-capped plug). The technology reaches the requirements of gigabit DRAM capacitors [14].

Trends in Capacitor Dielectrics for Gigabit DRAMs

First of all, the requirements of a capacitor dielectric in DRAM are briefly reviewed. Figure 1 shows a memory cell circuit. In a typical memory cell operation, the cell plate retains a half V_{CC}. To write, the level of V_S is set to 0 or V_{CC} by the bit line. To read, the bit line voltage, V_B, is precharged to a half V_{CC}, and then the polarity of the level shift in V_B, ΔV_B, is detected by a sense amplifier with a reference of a half V_{CC}. Conservation of electric charge gives

$$\Delta V_B = V_{CC}/[2(1 + C_B/C_S)]$$

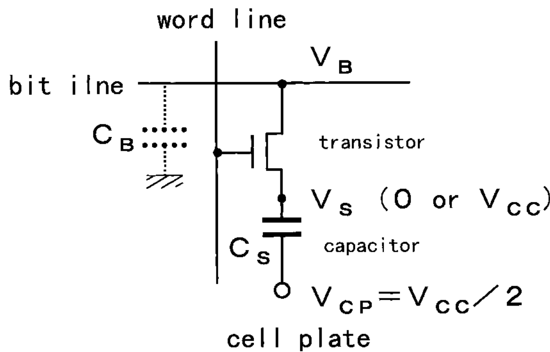

Fig. 1. Schematic Drawing of a DRAM memory cell circuit.

where C_S is a cell capacitance and C_B is a parasitic bit line capacitance. Let us assume that $V_{CC} = 2$ V, $C_B = 200$ fF, and the minimum ΔV_B (sensitivity of the sense amplifier) is 100 mV. Then C_S larger than 22 fF is required. Adding a margin to 22 fF, hereafter, we think that C_S should be 25 fF or more. The charge stored in the cell capacitor will decrease through leakage current during a refresh time. The refresh time will be 512 msec and a surface area of the storage node (see Fig. 2) will be less than 0.5 μm^2. Based on these estimations, simple calculation shows 10^{-6} A/cm^2 of the maximum allowable leakage current density for capacitor dielectrics when 10% loss of the storage charge ($= C_S V_{CC}/2$) is acceptable to operate the memory cell.

In the era of megabit DRAMs, cell capacitance has been kept in a tendency of very gradual decrease (despite the reduction in cell size) by applying higher dielectric constant silicon nitride (dielectric constant $\varepsilon_{Si_3N_4} = 7$, while $\varepsilon_{SiO_2} = 3.9$), decreasing the film thickness of the silicon nitride/oxide multi-layers, and increasing the surface area of the storage node relative to the reduced capacitor area by fabricating three-dimensional structures. Such developments are shown in the hemispherical grained (HSG) cylinder structure [28], the deep and narrow trench structure [29] and the

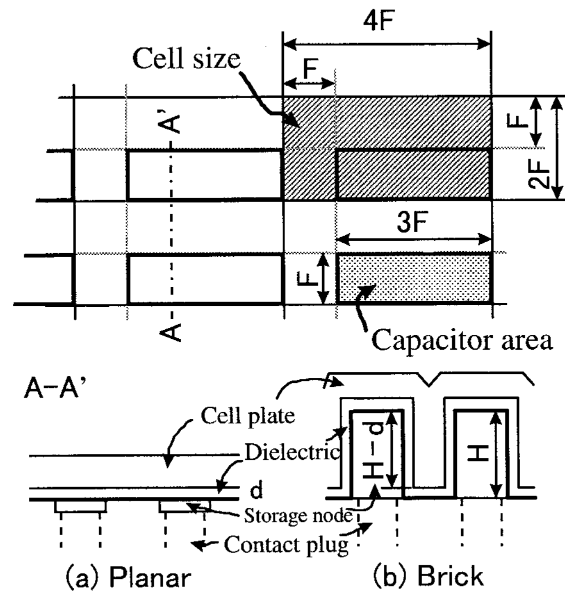

Fig. 2. 8F^2 arrangement of stacked capacitors in a capacitor over bit-line (COB) structure. F is a design rule and H is the height of a storage node.

high-aspect-ratio pillar structure [30], with an equivalent SiO_2 thickness of nearly 4 nm. The capacitors have essentially an SIS (S: poly-Si or Si substrate, I: dielectric) structure.

In the era of gigabit DRAMs, much higher dielectric constant materials are required to avoid further complex capacitor structures. One of the candidates for this purpose is Ta_2O_5 ($\varepsilon_{Ta_2O_5} = 20 - 25$) with a high stacked storage node [31–33]. Ta_2O_5 thin films have attained equivalent SiO_2 thickness of 2.5–3.5 nm with an MIS (M: metal, mostly TiN) structure [34–36] and that of 1.6 nm with an MIM (M: W for bottom electrode) structure [32,37,38]. With continuing emphasis on reducing cell size, however, a simple and lower stacked structure is required to ensure a wide process margin. It is expected, therefore, that gigabit DRAMs can be realized through a simple capacitor technology, involving the use of a higher dielectric constant material such as $(BaSr)TiO_3$ ($\varepsilon_{(BaSr)TiO_3} > 200$). $(BaSr)TiO_3$ is also applied in the MIM (M: RuO_2, Ru, Pt, TiN, etc.) structure to prevent formation of low-dielectric-constant SiO_2 on the semiconductor Si electrode.

Figure 2 shows an $8\,F^2$ arrangement of stacked capacitors in a capacitor over bit-line (COB) structure for a folded bit-line cell array. A simple stacked capacitor includes (a) planar and (b) brick structures. F is a design rule. H is the height of a storage node in the brick structure and d is a physical thickness of the dielectric film. Using a trend in the design rule for gigabit DRAMs, we can estimate required equivalent SiO_2 thicknesses in each structure fabricating a capacitance of 25 fF. The possibility to enlarge capacitor area by reducing the separation width is eliminated for the simplicity. The required equivalent SiO_2 thickness, with $H = 0$ (planar), F, 2F, 3F, is shown in Fig. 3 against the design rule. In the calculation, we ignore the thickness d which reduces an effective surface area of storage node, because d should be much smaller than F/2. Design rules of 0.18 μm, 0.13 μm and 0.09 μm may correspond to 1, 4 and 16 gigabit DRAMs, respectively.

CVD System and Characterization Procedure

Figure 4 (cited from [39]) illustrates a CVD system for the growth of Ba-Sr-Ti-O complex oxide using $Ba(thd)_2/Sr(thd)_2/Ti(O\text{-}i\text{-}C_3H_7)_4/O_2/Ar$ source compounds. thd is an abbreviation for a formal ligand name of 2,2,6,6-tetramethyl-3,5-heptanedionato and

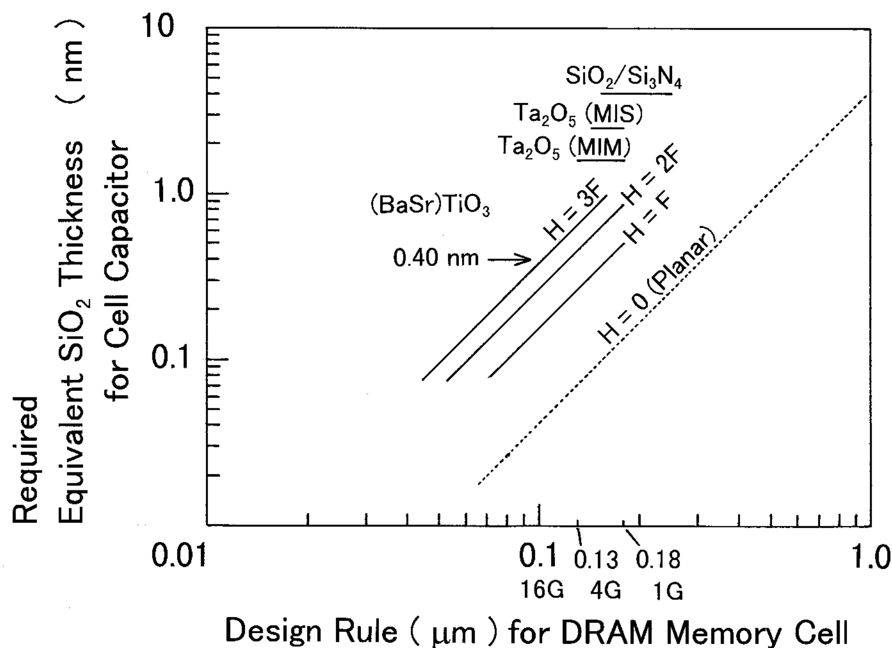

Fig. 3. Relationship between the required equivalent SiO_2 thickness and the design rule for DRAM memory cell. F: design rule, H: height of storage node. F may be 0.18 μm, 0.13 μm and 0.09 μm for 1 Gbit, 4 Gbit and 16 Gbit DRAMs, respectively.

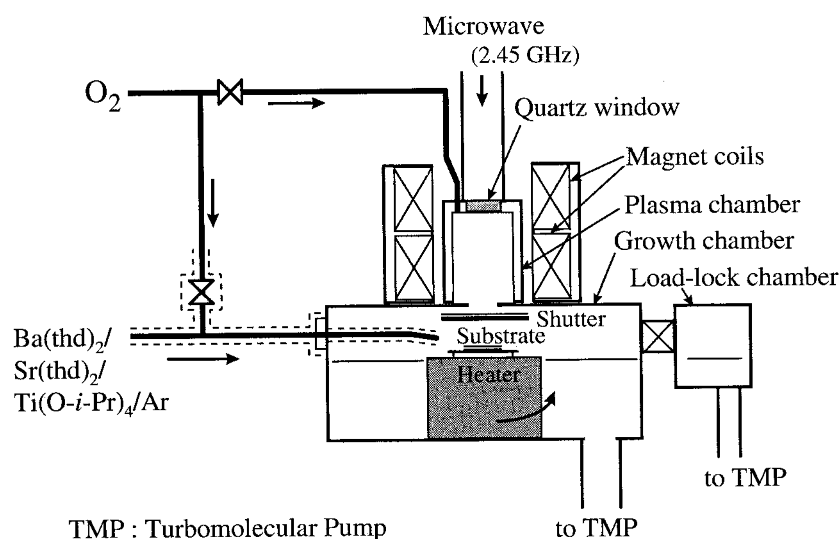

Fig. 4. Diagram of CVD system.

also called dipivaloylmethanato (DPM). When the system was operated with oxygen plasma, oxygen was introduced into the growth chamber through the plasma chamber. The system was also operated in a thermal CVD mode without oxygen plasma; in this case oxygen was introduced with source compounds. $Ti(O\text{-}i\text{-}C_3H_7)_4$ is a liquid and was vaporized at 20–36°C. $Ba(thd)_2$ and $Sr(thd)_2$ are solids and were sublimated at 175–205°C. Ar carrier gas flows transport source vapors into the growth chamber through gas lines heated at 220 ± 5°C. In our CVD system configuration, the deposition rate decreased steeply below 550°C without oxygen plasma [22].

Deposition conditions for $SrTiO_3$ and $(BaSr)TiO_3$ are summarized in Table I. ''Thermal CVD'' in the table means CVD process only with thermal energy. ECR plasma CVD, of course, uses a limited thermal energy. $Pt/TaO_x/Si$ substrates were prepared by annealing Pt/Ta/Si substrates at 600°C in O_2 atmosphere for 2 h. $Pt/R\text{-}Al_2O_3$ substrates were also annealed under the same condition for 1 h.

To measure the thicknesses of the films on the substrate electrodes, a surface profiler was used. Film compositions were determined by inductively coupled plasma atomic emission spectroscopy (ICP-AES), Rutherford backscattering spectroscopy (RBS) and energy dispersion of X-ray radiation (EDX) analysis. X-ray diffraction (XRD) was used to characterize the crystal structure of the films. Infrared reflection-absorption spectroscopy (IR-RAS) analysis were performed for detecting residual carbon. Carbon content in the films was determined using a $^{12}C^-/^{18}O^-$ ratio measured by secondary ion mass spectroscopy (SIMS) and the ^{18}O natural abundance

Table 1. Deposition conditions in thermal and ECR plasma CVD for $SrTiO_3$ and $(BaSr)TiO_3$.

	Thermal CVD	ECR plasma CVD	
	$SrTiO_3$	$SrTiO_3$	$(BaSr)TiO_3$
Total pressure	75 Pa	1 Pa	1 Pa
Deposition temperature	600°C	450 ~ 650°C	450 ~ 500°C
Microwave power	—	580 W	750 W
Deposition rate	0.5 ~ 1.0 nm/min	1 nm/min	1.0 ~ 1.1 nm/min
Substrate electrode	Pt / TaO_x / Si	Pt / $R\text{-}Al_2O_3$	Pt / TaO_x / Si
Top electrode	Au	Au	Al / TiN

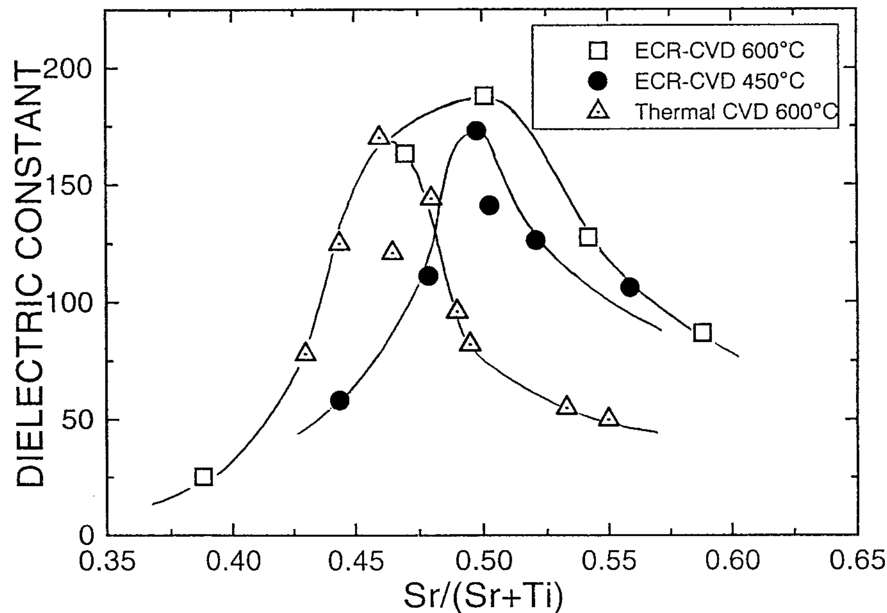

Fig. 5. Dependence of the dielectric constant on Sr/(Sr + Ti) of the $SrTiO_3$ films. Film thicknesses are 90–120 nm.

of 0.2%. Dielectric constants were calculated on the basis of capacitance measured at 10 kHz at room temperature.

Investigation on $SrTiO_3$ Films by CVD

Effect of Oxygen Plasma on Crystallization and Carbon Contamination

To investigate features of ECR plasma CVD for a low temperature deposition method, $SrTiO_3$ films were characterized. Figure 5 (cited from [39]) shows the relationship between dielectric constant and film composition, Sr/(Sr + Ti). In thermal CVD at 600°C and at a film composition of 0.50, the dielectric constant was 80, while it reached a maximum of 170 at 0.46. This indicates that the rate of perovskite phase ($SrTiO_3$) formation increases in the presence of excess TiO_x. In ECR plasma CVD at 600°C, however, the maximum dielectric constant occurred at 0.50 and was 190. A comparison of the two curves clearly shows that oxygen plasma enhances the formation of perovskite. In ECR plasma CVD, $SrTiO_3$ films with a maximum dielectric constant of 170 were obtained at the low growth temperature of 450°C. Figure 6 (cited from [40]) also shows that the crystallization was not completed in $SrTiO_3$ films by the thermal CVD. Through the annealing in an oxygen ambient at 600°C for 2 h, dielectric constants of $SrTiO_3$ films greatly improved.

It is also discussed that the grain size in $SrTiO_3$ films is affected by the microwave power in ECR

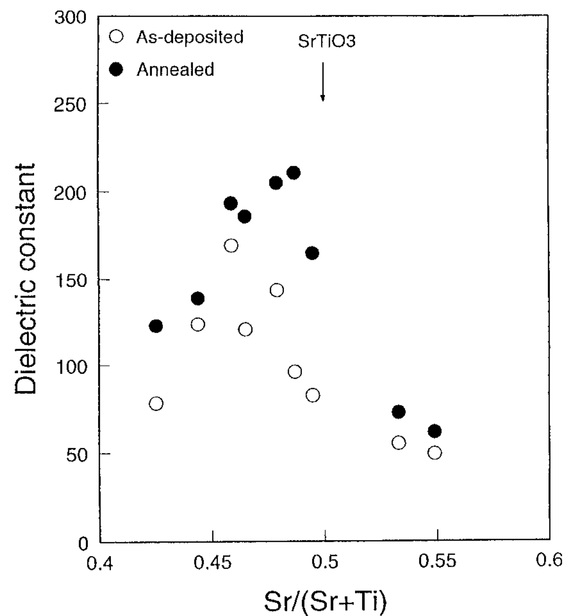

Fig. 6. Dependence of the dielectric constant on Sr/(Sr + Ti) of the $SrTiO_3$ films by thermal CVD.

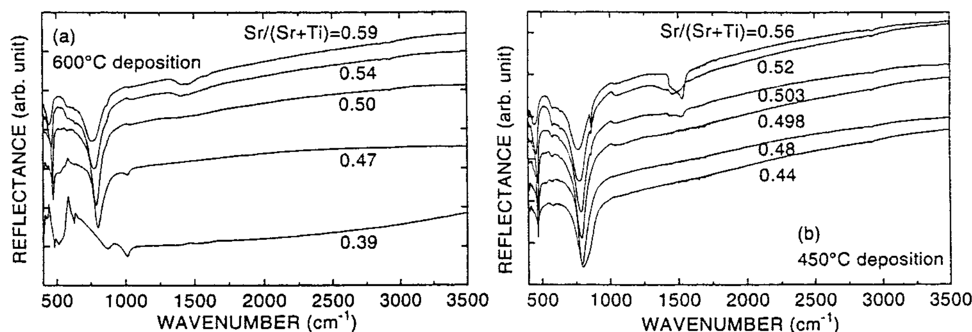

Fig. 7. Infrared reflection-absorption spectra of the $SrTiO_3$ films grown at (a) 600°C and (b) 450°C.

plasma CVD [41]. The grain size increased as the microwave power increased, probably because excited oxygen atoms enhance the migration of Sr ions. The higher microwave power resulted in good electrical properties of higher dielectric constant and lower leakage current density. The oxygen plasma may improve the crystallinity of grains and grain boundaries in $SrTiO_3$ films. Another example to show the effect of oxygen plasma on crystallization (and excitation of source compounds) is seen in the ECR plasma CVD of $YBa_2Cu_3O_x$ superconducting thin films [42].

IR-RAS spectra from $SrTiO_3$ films by ECR plasma CVD are shown in Fig. 7 (cited from [43]). Absorption at around $1400\,cm^{-1}$ is related to the uncrystalline carbonate [44]. This absorption depends essentially on the composition Sr/(Sr + Ti). In the Sr-rich $SrTiO_3$ films the carbonate remains. Figure 8 (cited from [39]) shows carbon content in the films, measured as $^{12}C^-/^{18}O^-$ by SIMS. A $^{12}C^-/^{18}O^-$ ratio of 1.0 means 0.6 mole-% of C-containing phase, which is most probably a carbonate ($SrCO_3$). The carbonate formation is strongly related to the excess Sr in the films. The effect of oxygen plasma in reducing the carbon contamination [45] was confirmed also in this study, since carbon content was smaller in the films grown by ECR plasma CVD. The carbon content increased with decreasing growth temperature in ECR plasma CVD.

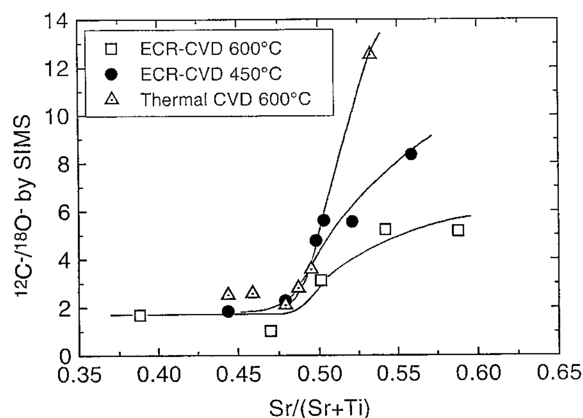

Fig. 8. Carbon content in the $SrTiO_3$ films against the film composition Sr/(Sr + Ti). Carbon contents are represented by $^{12}C^-/^{18}O^-$ measured in SIMS.

In a Sr-rich film composition, a $SrTiO_3$ phase of cubic structure changed to a $(SrTiO_3)_m(SrO)_n$ phase of tetragonal superstructure [40]. This change was revealed by the shifts of XRD peaks related to 001, 101, and 002 reflections toward the lower diffraction angle in 2θ. Figure 9 (cited from [39]) shows measured 002 plane distance, which corresponds to the 0 0 2m + n plane distance in $(SrTiO_3)_m(SrO)_n$ [m > n], with respect to the Sr/(Sr + Ti) ratio of the film. The broken line connects data points for $SrTiO_3$[1.952 Å], $Sr_4Ti_3O_{10}$[2.011 Å], $Sr_3Ti_2O_7$[2.04 Å], and Sr_2TiO_4[2.099 Å]. At the low temperature of 450°C, TiO_x phase is readily

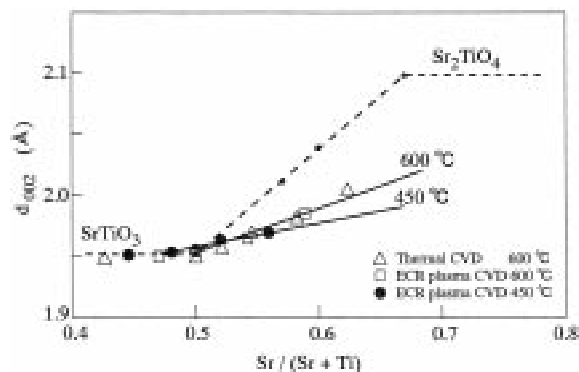

Fig. 9. 002 related plane distance against the film composition Sr/(Sr + Ti).

formed. This TiO_x formation makes a remaining part Sr-rich and the enlargement of 002 plane distance takes place in the range from slightly Ti-rich to Sr-rich compositions [43]. An n/m of the superstructure was greater in the film grown at 600°C. In Fig. 9, we can see that the solid lines are below the broken line, which means that all excess SrO does not form the superstructure. The formation of superstructure is a thermal process and the oxygen plasma does not affect the process.

$(BaSr)TiO_3$ Films for Gigabit DRAM Capacitor Application

The film composition is important to obtain the higher dielectric constant and the lower leakage current density. The $(BaSr)TiO_3$ composition with (Ba + Sr)/Ti = 0.97 and Ba/(Ba + Sr) = 0.4 was selected to apply the films for gigabit DRAM capacitors [27].

The deposition rate relates strongly to the chemical potential difference between the gas phase and the film. And the ratio of the surface migration flux to the site-incorporation flux is made higher by the lower chemical potential difference at the gas-solid interface. Therefore, the deposition rate is an effective parameter to improve film properties. This is also discussed in CVD of Bi-Sr-Ca-Cu-O ultrathin films [46]. Figure 10 (cited from [47]) shows that grain size and dielectric constant increase as deposition rate

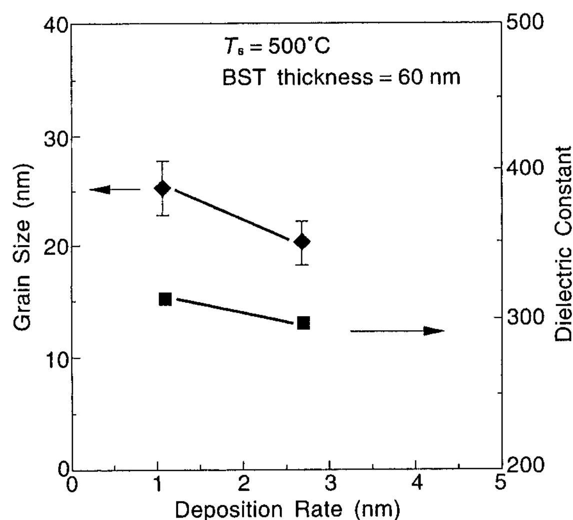

Fig. 10. Effect of the deposition rate on the $(BaSr)TiO_3$ film properties.

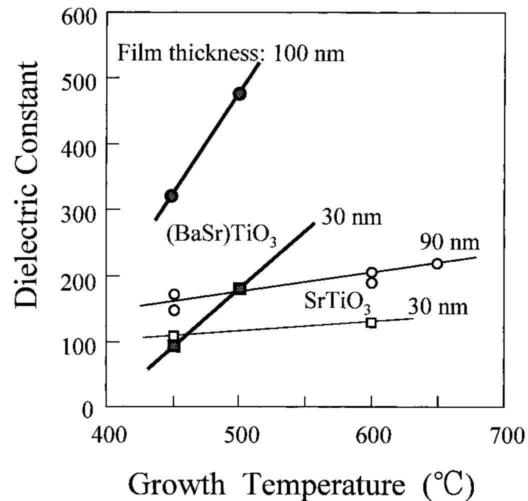

Fig. 11. Dependence of $(BaSr)TiO_3$ and $SrTiO_3$ dielectric constant on deposition temperature.

decreases [27]. Thus the lower deposition rate of 1.1 nm/min was selected.

Figure 11 (cited from [39]) shows the dependence of $SrTiO_3$ and $(BaSr)TiO_3$ dielectric constants on deposition temperature. The dielectric constant increases as the deposition temperature increases. In the integration to cell capacitors, $(BaSr)TiO_3$ was deposited at 550°C to obtain the higher dielectric constant. The dielectric constant depends also on the film thickness. More important is that the selection of top electrode materials affects the dielectric constant measured [48]. Ru was selected for the top electrode of integrated capacitors.

The step coverage observed in the secondary electron microscopy (SEM) cross-section is shown in Fig. 12 with illustrations (cited from [48]), where 100 nm thick $SrTiO_3$ layers were deposited on the SiO_2 steps with a 0.5 μm height and a 0.5 μm spacing. Figure 12(a) shows a step coverage by thermal CVD at 1 Pa and 600°C and Fig. 12(b) shows that by ECR plasma CVD at 1 Pa and 450°C. In Fig. 12(a) for thermal CVD, the sidewall deposition at the top was thicker than that at the bottom, which implies a higher sticking probability compared with the probability in the conformal CVD system. In contrast, the thickness on the sidewall was uniform from the top to the bottom in ECR plasma CVD, as shown in Fig. 12(b), presumably because the plasma flow has a directionality vertical to the substrate surface.

Composition distribution of BST films on the simple stacked electrode (made of RuO_2) is shown in

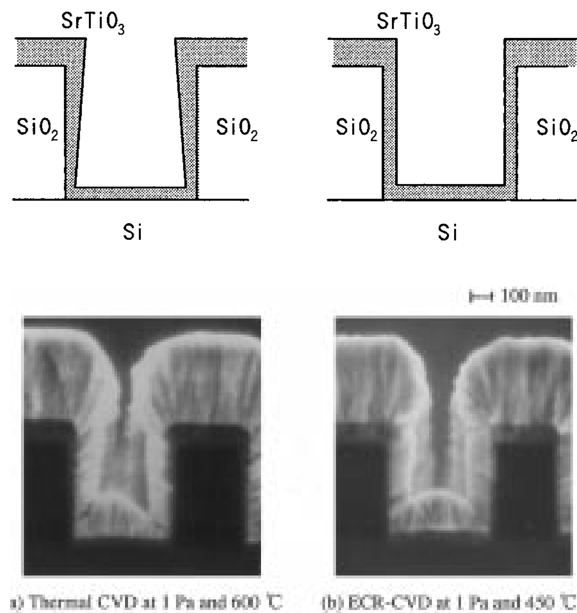

Fig. 12. SEM cross sections showing the step coverage of 100 nm (on top) thick $SrTiO_3$ (gray) layers on SiO_2 (black) lines with a 500 nm height and a 500 nm spacing. The $SrTiO_3$ layers are covered with thick Ta (white) overlayers for SEM observation. The 100 nm scale is for the photographs. Illustrations display the $SrTiO_3$ coverages. The Ta overlayers are not shown in the illustrations. (a) Thermal CVD, (b) ECR plasma CVD.

Fig. 13 (cited from [47]). The stack height was 0.65 μm and the spacing was 0.60 μm. The $(BaSr)TiO_3$ film thickness on the top surface was 95 nm, and 40 nm on the sidewall. The Ba:Sr:Ti:O compositions of eight points shown in the inset were measured by cross-sectional transmission electron microscopy (TEM)-EDX analysis with an electron beam size of 1 nmϕ. When Ba + Sr composition was set at 1.00, average composition of the top surface positions (1–2) was Ba:Sr:Ti:O = 0.44:0.56:0.94:2.87 and that of the sidewall positions (5–8) was 0.47:0.53:1.01:3.05. The composition of $(BaSr)TiO_3$ film deposited under the same conditions was Ba:Sr:Ti = 0.40:0.60:1.02 measured by RBS. The difference between the measured compositions by EDX and RBS may originate from the systematic error in EDX measurement. In Fig. 13, the thin lines show the standard deviations of Ba, Sr and Ti composition measurements. Considering the composition measurement with the deviation, it should be noted that the $(BaSr)TiO_3$ compositions on the electrode top surface and sidewall are uniform within a deviation of $\pm$ 14% for Sr.

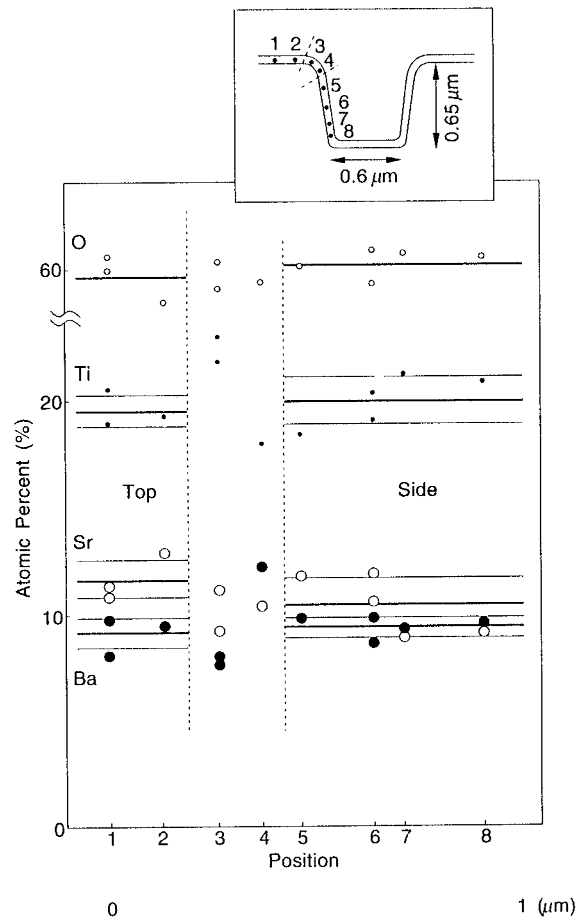

Fig. 13. Composition distribution in a $(BaSr)TiO_3$ film over the patterned RuO_2 node.

Integration of $(BaSr)TiO_3$ in the DRAM Cell Capacitor

It is reported that the array of Pt storage nodes was formed using a fabrication process of larger than a quarter micrometer [49,50]. However, below 0.2 μm process is necessary for gigabit DRAM applications. Therefore RuO_2/Ru storage nodes have been developed [51]. Based on the study of degradation of barrier layers between RuO_2 and Si in an oxidizing atmosphere [52], the barrier structure with high endurance against oxidation was developed. Figure 14 shows the fabrication process flow for the cell capacitor with $(BaSr)TiO_3$ dielectric thin film over the stacked RuO_2/Ru storage node contacting a TiN/$TiSi_x$/poly-Si plug [14]. A schematic cross-

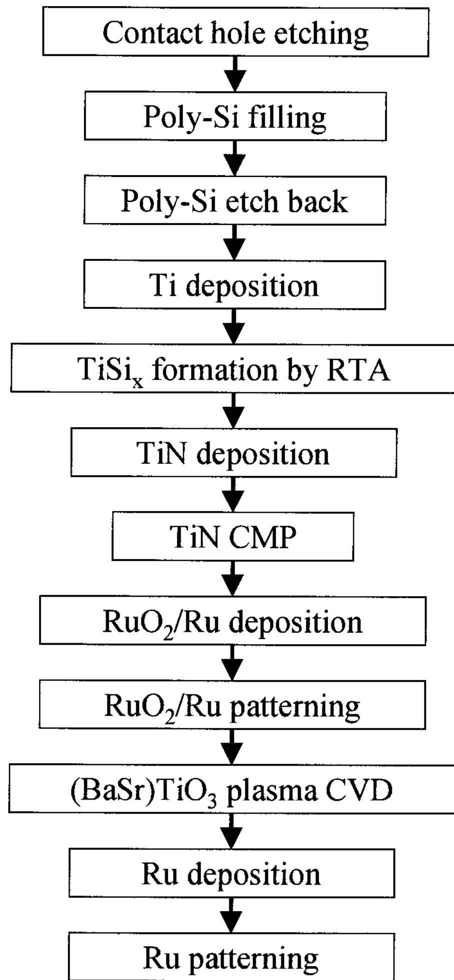

Fig. 14. Flow chart of the $(BaSr)TiO_3$ cell capacitor fabrication process.

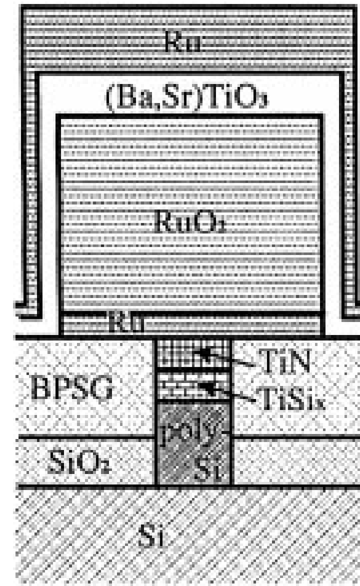

Fig. 15. Schematic cross section of the $Ru/(BaSr)TiO_3/RuO_2/Ru$ capacitor with a $TiN/TiSi_x$/poly-Si plug.

section of the capacitor is shown in Fig. 15 (cited from [48]).

At first $0.15\,\mu m\phi$ contact holes were formed through 200 nm boro-phospho silicate glass (BPSG) over 100 nm SiO_2 by electron beam (EB) lithography and reactive ion etching (RIE). The contact holes were then filled with phosphorus-doped poly-Si (DOPOS). Blanket deposition of DOPOS was etched back until DOPOS surface in the contact hole is recessed from BPSG surface by 100 nm. Ti and TiN deposition method was dc sputtering using a Ti metal target with an Ar pure gas and an Ar/N_2 gas mixture, respectively. First, Ti was deposited and rapidly annealed (RTA) in N_2 ambient to form $TiSi_x$ in the holes. Then TiN filled the holes and the surface was planarized by chemical mechanical polishing (CMP) to remove TiN on the BPSG and form buried-in $TiN/TiSi_x$/poly-Si plugs.

50 nm Ru and 400 nm RuO_2 were deposited by dc sputtering using a Ru metal target with sputtering gas of Ar and Ar/O_2, respectively. To pattern the storage node of RuO_2/Ru contacting the $TiN/TiSi_x$/poly-Si plug, spin on glass (SOG) hard mask on RuO_2 was patterned by EB lithography and reactive ion etching (RIE) using CHF_3. Then RuO_2/Ru storage nodes were fabricated by RIE using an O_2/Cl_2 gas mixture [53]. SOG mask was removed by wet etching with a buffered HF solution. The RuO_2/Ru storage nodes with a spacing of $0.15\,\mu m$ and a height of $0.45\,\mu m$ were fabricated. A cell size and a capacitor area were $0.67 \times 0.33\ (=0.23)\ \mu m^2$ and $0.52 \times 0.18\ (=0.094)\ \mu m^2$, respectively. No oxidation of TiN and $TiSi_x$ in the contact hole was observed by EDX analysis after annealing the RuO_2/Ru storage node in an oxygen plasma at 550°C [14].

$(BaSr)TiO_3$ thin films were prepared on the RuO_2/Ru storage nodes at 550°C with a deposition rate of 1.1 nm/min by the ECR plasma CVD described in the previous sections. Dielectric film compositions were $(Ba+Sr)/Ti = 0.97$ and $Ba/(Ba+Sr) = 0.4$. Finally, a top electrode (cell plate) of 200 nm thick Ru was deposited by dc sputtering. Ru cell plate was patterned by RIE with an SOG hard

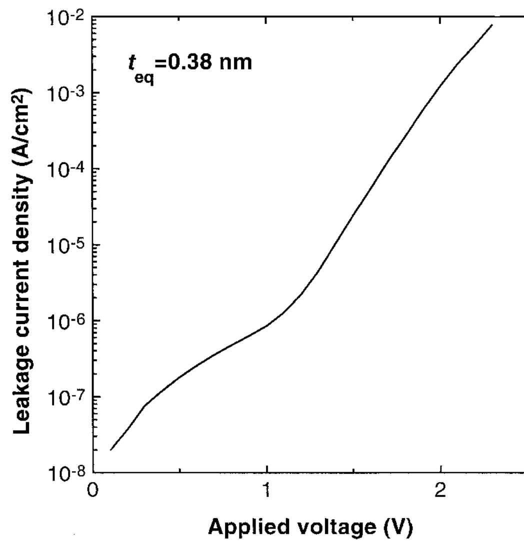

Fig. 16. Leakage current density of 30 nm-thick $(BaSr)TiO_3$ film.

mask.

Under the same CVD condition, 30 nm thick $(BaSr)TiO_3$ showed an equivalent SiO_2 thickness of 0.38 nm in the capacitor structure of top-Ru/$(BaSr)TiO_3$/bottom-RuO_2. A leakage current density was 8.5×10^{-7} A/cm^2 at 1.0 V and shown in Fig. 16 (cited from [48]). An equivalent SiO_2 thickness of $(BaSr)TiO_3$ on the RuO_2 sidewall was evaluated from the slope of the relation between sum of cell capacitances and sum of sidewall areas. On the sidewalls of the storage nodes, an equivalent SiO_2 thickness of 0.40 nm was obtained. Using dielectric films of 0.40 nm equivalent SiO_2 thickness, cell capacitors for gigabit DRAMs can be fabricated with an appropriate height of storage nodes (see Fig. 3).

Conclusion

The $(BaSr)TiO_3$ integration technology required for use of these dielectric thin films for capacitors in the gigabit DRAM memory cell, were satisfied with the low process temperature. A thin $(BaSr)TiO_3$ film produced by ECR plasma CVD showed adequate electrical properties at this low deposition temperature, 550°C, without any further annealing. A buried-in TiN/$TiSi_x$/poly-Si plug under the RuO_2/Ru storage node endured against oxidation during the $(BaSr)TiO_3$ deposition. An equivalent SiO_2 thickness of $(BaSr)TiO_3$ films decreased to 0.38 nm and the leakage current density was below 10^{-6} A/cm^2 at an applied voltage of 1.0 V. An equivalent SiO_2 thickness of 0.40 nm on the RuO_2 sidewall was also achieved. This technology satisfies the requirements for the gigabit DRAM capacitors.

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